What is claimed is:

1. A memory device, comprising:

a substrate having a source region;

a nanotube array including a plurality of nanotube columns that are vertically grown on the substrate such that a first end of the nanotube array is in contact with the source region, the nanotube array functioning as an electron transport channel;

a memory cell formed around an outer side surface of the nanotube array;

a control gate formed around an outer side surface of the memory cell; and

a drain region in contact with a second end of the nanotube array and the memory cell, wherein the second end of the nanotube array is distal to the first end of the nanotube array.

2. The memory device as claimed in claim 1, wherein the substrate is made of one material selected from the group consisting of aluminum oxide, silicon, and a mesoporous material.

3. The memory device as claimed in claim 1, wherein the plurality of nanotube columns are made of one material selected from the group consisting of carbon, boronitride, and gallium phosphate.

4. The memory device as claimed in claim 1, wherein the memory cell comprises:

a first insulation layer formed around the outer side surface of the nanotube array;

an electron storing layer formed around an outer side surface of the first insulation layer; and

a second insulation layer formed around an outer side surface of the electron storing layer to be in contact with the control gate.

5. The memory device as claimed in claim 4, wherein the first insulation layer and the second insulation layer are silicon oxide layers.

6. The memory device as claimed in claim 4, wherein the electron storing layer is a silicon layer or a silicon nitride layer.

7. The memory device as claimed in claim 1, wherein the memory cell has a thickness of less than about 200 nm.

8. The memory device as claimed in claim 4, wherein the electron storing layer has a thickness of about 100 nm or less.

9. The memory device as claimed in claim 4, wherein the electron storing layer is a porous layer including a plurality of nanodots, each of the plurality of nanodots being filled with an electron storing material.

10. The memory device as claimed in claim 9, wherein the electron storing material is one of silicon and silicon nitride.

11. The memory device as claimed in claim 9, wherein the porous layer is an aluminum oxide layer.

12. The memory device as claimed in claim 9, wherein the nanodots have a diameter of about 100 nm or less.

13. The memory device as claimed in claim 10, wherein the nanodots have a diameter of about 100 nm or less.

14. The memory device as claimed in claim 11, wherein the nanodots have a diameter of about 100 nm or less.